CLAIMS

What is claimed is:

1. A method for thinning a semiconductor wafer, comprising:

providing a semiconductor wafer having a circuitized active surface and a backside surface;

securing and supporting the semiconductor wafer in a substantially unwarped state on a fixture;

and, while maintaining the semiconductor wafer in the substantially unwarped state:

backgrinding the backside surface to a selected thickness;

applying material to the backside surface to penetrate recesses in topography thereof and adhere thereto; and

hardening the material to a solid state exhibiting a substantially planar exposed surface and bonded to the backside surface; and

releasing the semiconductor wafer from the fixture.

2. The method of claim 1, further comprising applying the material to the backside surface without polishing thereof from a rough-ground state.

3. The method of claim 1, further comprising selecting the material to have, in the solid state, a coefficient of expansion at least as great as a coefficient of thermal expansion of the semiconductor wafer.

4. The method of claim 1, wherein backgrinding is conducted with one of abrasion and chemically enhanced abrasion.

5. The method of claim 1, further comprising backgrinding to produce a backside surface having a mean surface roughness factor R_a of between about 5% and about 40% of a mean selected thickness of the back-ground semiconductor wafer.

6. The method of claim 1, further comprising backgrinding to produce a backside surface having a mean surface roughness factor R_a of between about 2 μm and about 15 μm.

7. The method of claim 1, further comprising selecting the material to comprise a dielectric material.

8. The method of claim 1, further comprising selecting the material to comprise a polymer.

9. The method of claim 1, further comprising selecting the material to comprise at least one of the polymer groups comprising epoxies, acrylics, silicones, urethanes, siloxanes and Parylenes™.

10. The method of claim 1, further comprising selecting the material to comprise one of a thermoset cross-linkable polymer, a UV cross-linkable polymer and a two-part epoxy.

11. The method of claim 1, further comprising forming the material as an epoxy film cured to a "B" stage of tackiness and applied to the backside surface, and heating the epoxy film to complete curing thereof.

12. The method of claim 1, further comprising applying the material as a Parylene™ by:

heating a dimer to form vaporized monomers thereof; and

contacting the monomers with the backside surface at a lower temperature and reduced pressure to form a polymer layer thereon.

13. The method of claim 1, further comprising selecting the material to comprise an ionic barrier.

14. The method of claim 1, wherein the material is a flowable material and further comprising applying the material by one of dispensing, screen-coating, stencil-coating, and spin-coating.

15. The method of claim 1, wherein the material is at least a semisolid element and applying comprises laminating the at least a semisolid element to the backside surface.

16. The method of claim 15, wherein the at least a semisolid element comprises one of a tape and film.

17. The method of claim 15, wherein the at least a semisolid element comprises a layer of the material placed on a backing layer, and applying comprises applying the layer of the material to the backside surface and removing the backing layer.

18. The method of claim 17, further comprises applying a release layer to the backing layer before placing the material thereon, and removing the backing layer comprises releasing the layer of the material from the backing layer using the release layer.

19. The method of claim 1, further comprising singulating the semiconductor wafer with the hardened material adhered to the backside surface into a plurality of discrete semiconductor dice.

20. The method of claim 1, further comprising selecting a material for the semiconductor wafer from silicon, gallium arsenide, germanium and indium phosphide.

21. The method of claim 1, further comprising backgrinding the semiconductor wafer to a selected thickness of about 10 mils (about 254 μm) or less.

22. The method of claim 1, further comprising backgrinding the semiconductor wafer to a selected thickness of about 4 mils (about 102 μm) or less.

23. The method of claim 1, further comprising backgrinding the semiconductor wafer to a selected thickness of about 2 mils (about 51 μm) or less.

24. The method of claim 1, further comprising applying the material in sufficient quantity to provide a level of the material on the backside surface at least equal to a level of a highest peak on the backside surface.

25. The method of claim 1, further comprising applying the material in sufficient quantity to form a substantially planar exposed surface at a level of up to about 100 μm above a level of a highest topographic feature on the backside surface.

26. The method of claim 1, further comprising applying the material in sufficient quantity to form a substantially planar exposed surface at a level of up to about 10 μm above a level of a highest topographic feature on the backside surface.

27. A semiconductor wafer having an active surface and a backside surface and including a plurality of semiconductor dice formed thereon, wherein:
the active surface includes integrated circuitry thereon;
the backside surface is in a back-ground state;
a solid material extends over and is bonded to the backside surface; and
an interface between the backside surface and the solid material has a mean surface roughness factor R_a of between about 5% and about 40% of a mean thickness of the semiconductor wafer.

28. The semiconductor wafer of claim 27, wherein semiconductor material of the semiconductor wafer comprises one of silicon, gallium arsenide, germanium and indium phosphide.

29. The semiconductor wafer of claim 27, wherein the interface has a mean surface roughness factor R_a between about 2 μm and about 15 μm.

30. The semiconductor wafer of claim 27, wherein the solid material comprises a polymer.

31. The semiconductor wafer of claim 27, wherein the solid material includes at least one of the polymer groups comprising epoxies, acrylics, silicones, urethanes, siloxanes and Parylenes™.

32. The semiconductor wafer of claim 27, wherein the solid material comprises one of a thermoset cross-linkable polymer, a UV cross-linkable polymer and a two-part epoxy.

33. The semiconductor wafer of claim 27, wherein the solid material comprises a Parylene™ polymer.

34. The semiconductor wafer of claim 27, wherein the solid material has a mean thickness of about 100 μm or less over a highest topographic feature on the backside surface.

35. The semiconductor wafer of claim 27, wherein the solid material has a mean thickness of about 10 μm or less over a highest topographic feature on the backside surface.

36. The semiconductor wafer of claim 27, wherein the solid material has a generally planar exposed surface.

37. The semiconductor wafer of claim 27, wherein the solid material comprises an ionic barrier.

38. The semiconductor wafer of claim 27, wherein the semiconductor wafer has a thickness of about 4 mils or less.

39. The semiconductor wafer of claim 27, wherein the semiconductor wafer has a thickness of about 2 mils or less.

40. The semiconductor wafer of claim 27, wherein the semiconductor wafer has a nominal diameter of at least about 200 mm (about 8 inches).

41. The semiconductor wafer of claim 27, wherein the semiconductor wafer has a nominal diameter of at least about 300 mm (about 12 inches).

42. The semiconductor wafer of claim 27, wherein material of the semiconductor wafer is in a state of compression.

43. A semiconductor package, comprising:

a die of semiconductor material having an active surface and a backside surface;

integrated circuitry on the active surface;

wherein the backside surface is in a roughly back-ground state and includes a solid material extending thereover and bonded thereto;

a protective material encapsulating at least a portion of the die and the solid material extending over the backside surface; and

a plurality of conductive terminals exposed through the protective material on a surface of the package;

wherein an interface between the backside surface and the solid material has a mean surface roughness factor R_a of between about 5% and about 40% of the mean thickness of the die.

44. The package of claim 43, wherein the interface has a mean surface roughness factor R_a of between about 2 μm and about 15 μm.

45. The package of claim 43, wherein the solid material comprises a polymer.

46. The package of claim 43, wherein the solid material includes at least one of the polymer groups comprising epoxies, acrylics, silicones, urethanes, siloxanes and Parylenes™.

47. The package of claim 43, wherein the solid material comprises one of a thermoset cross-linkable polymer, a UV cross-linkable polymer and a two-part epoxy.

48. The package of claim 43, wherein the solid material comprises a Parylene™ polymer.

49. The package of claim 43, wherein the semiconductor material of the die is in a state of compression.

50. A semiconductor wafer having a thickness of about 4 mils or less and which maintains an unwarped state in an absence of external force applied thereto.

51. The semiconductor wafer of claim 50, wherein the thickness is about 2 mils or less.

52. The semiconductor wafer of claim 50, wherein material of the semiconductor wafer is in a state of compression.